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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,906	11/26/2003	Wolfgang Hetzel	MAS-FIN-419	1149

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,906	HETZEL ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-11* is/are pending in the application.

4a) Of the above claim(s) *10 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (PN 6,087,718, of record) in view of Lin et al. (PN 6,593,649).

Cho discloses, as shown in Figure 2, an electronic component, comprising:

a chip stack including a first semiconductor chip (5) having an active surface and a second semiconductor chip (7) having an active surface;

a plurality of flat conductors (2), each one of the plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section, the inner section of each one of the plurality of flat conductors and the central section of each one of the plurality of flat conductors configured between the first semiconductor chip and the second semiconductor chip;

a package;

a plurality of first bonding connections (9);

a plurality of second bonding connections (9);

the first semiconductor chip having a plurality of contact surfaces;

the second semiconductor chip having a plurality of contact surfaces;

each one of the plurality of first bonding connections connecting one of the plurality of contact surfaces on the first semiconductor chip to the inner section of one of the plurality of flat conductors;

each one of the plurality of second bonding connections connecting one of the plurality of contact surfaces on the second semiconductor chip to the transitional section of one of the plurality of flat conductors.

Cho does not disclose a first interposer layer or interposer film configured on the active surface of the first semiconductor chip, the first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces and a second interposer layer or interposer film configured on the active surface of the second semiconductor chip, the second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces. However, Lin et al. discloses an electronic component comprising an interposer layer or interposer film (13,18,40) configured on the active surface of the semiconductor chip, the interposer layer or interposer film having bonding fingers, interposer lines and bonding surfaces. Note Figures 1-5 of Lin et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the component of Cho having an interposer layer or interposer film configured on the active surface of the semiconductor chip, the interposer layer or interposer film having bonding fingers, interposer lines and bonding surfaces, such as taught by Lin et al. in order to allow the input/output pads location for the packaging of semiconductor devices of different dimensions while using more universal package and to enhance the reliability of wire bond operations.

Regard claim 2, Cho and Lin et al. disclose one of the plurality of first bonding connections is connected to the inner section of a given one of the plurality of flat conductors; and

one of the plurality of second bonding connections is connected to the transitional section of the given one of the plurality of flat conductors.

Regard claim 4, Cho and Lin et al. disclose the first semiconductor chip includes a bonding channel and the second semiconductor chip includes a bonding channel congruently configured with respect to the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the first semiconductor chip are configured in the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the second semiconductor chip are configured in the bonding channel of the second semiconductor chip

Regard claim 6, Cho and Lin et al. disclose the active surface of the first semiconductor chip is mounted on the central section of each one of the plurality of flat conductors; and

the active surface of the second semiconductor chip is mounted on the central section of each one of the plurality of flat conductors.

Regard claim 8, Cho and Lin et al. disclose the outer section of each one of the plurality of flat conductor has a z-shaped bend aligned such that the active surface of the first semiconductor chip and the active surface of the second semiconductor chip are aligned in a direction opposite the bends.

2. Claims 1 – 4 and 6 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (PN 6,483,181, of record) in view of Lin et al. (PN 6,593,649).

Chang et al. discloses, as shown in Figures 2 and 4, an electronic component, comprising:

a chip stack including a first semiconductor chip (210) having an active surface and a second semiconductor chip (220) having an active surface;

a plurality of flat conductors (230), each one of the plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section, the inner section of each one of the plurality of flat conductors and the central section of each one of the plurality of flat conductors configured between the first semiconductor chip and the second semiconductor chip;

a package;

a plurality of first bonding connections (270);

a plurality of second bonding connections (270);

the first semiconductor chip having a plurality of contact surfaces;

the second semiconductor chip having a plurality of contact surfaces;

each one of the plurality of first bonding connections connecting one of the plurality of contact surfaces on the first semiconductor chip to the inner section of one of the plurality of flat conductors;

each one of the plurality of second bonding connections connecting one of the plurality of contact surfaces on the second semiconductor chip to the transitional section of one of the plurality of flat conductors.

Chang et al. does not disclose a first interposer layer or interposer film configured on the active surface of the first semiconductor chip, the first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces and a second interposer layer or interposer film configured on the active surface of the second semiconductor chip, the second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces. However, Lin et al. discloses an electronic component comprising an interposer layer or interposer film (13,18,40) configured on the active surface of the semiconductor chip, the interposer layer or interposer film having bonding fingers, interposer lines and bonding surfaces. Note Figures 1-5 of Lin et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the component of Chang et al. having an interposer layer or interposer film configured on the active surface of the semiconductor chip, the interposer layer or interposer film having bonding fingers, interposer lines and bonding surfaces, such as taught by Lin et al. in order to allow the input/output pads location for the packaging of semiconductor devices of different dimensions while using more universal package and to enhance the reliability of wire bond operations.

Regard claim 2, Chang et al. and Lin et al. disclose one of the plurality of first bonding connections is connected to the inner section of a given one of the plurality of flat conductors; and

one of the plurality of second bonding connections is connected to the transitional section of the given one of the plurality of flat conductors.

Regard claim 3, Chang et al. and Lin et al. disclose the plurality of first bonding surfaces on the first interposer layer or interposer film and the plurality of second bonding surfaces on the second interposer layer or interposer film are configured at mutually congruent positions. Note that since the same interposer layer or interposer film is applied to both the first and second chip, it is inherent that the plurality of first bonding surfaces and the plurality of second bonding surfaces are configured at mutually congruent positions

Regard claim 4, Chang et al. and Lin et al. disclose discloses the first semiconductor chip includes a bonding channel and the second semiconductor chip includes a bonding channel congruently configured with respect to the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the first semiconductor chip are configured in the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the second semiconductor chip are configured in the bonding channel of the second semiconductor chip

Regard claim 6, Chang et al. and Lin et al. disclose the active surface of the first semiconductor chip is mounted on the central section of each one of the plurality of flat conductors; and

the active surface of the second semiconductor chip is mounted on the central section of each one of the plurality of flat conductors.

Regard claim 7, Chang et al. and Line et al. disclose the outer section of each one of the plurality of flat conductor has a z-shaped bend aligned such that the active surface of the first

semiconductor chip and the active surface of the second semiconductor chip are aligned in a direction of the bends.

Regard claim 8, Chang et al. and Lin et al. disclose the outer section of each one of the plurality of flat conductor has a z-shaped bend aligned such that the active surface of the first semiconductor chip and the active surface of the second semiconductor chip are aligned in a direction opposite the bends.

Regard claim 9, Chang et al. and Lin et al. disclose the transitional section of each one of the plurality of flat conductors has a bend toward the active surface of the second semiconductor chip.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (PN 6,087,718, of record) in view of Lin et al. (PN 6,593,649) and further in view of Chang et al. (PN 6,483,181, of record).

Cho and Lin et al. disclose the claimed invention including the electronic component as recited in the rejection above. Cho and Lin et al. do not disclose the active upper face of the first

semiconductor chip and the active upper face of the second semiconductor chip are aligned in direction of the bend or bond toward the active upper face of the second semiconductor chip. However, Chang et al. discloses the active upper face of the first semiconductor chip and the active upper face of the second semiconductor chip are aligned in direction of the bend or opposite the bend or bond toward the active upper face of the second semiconductor chip. Note Figures 2 and 4 of Chang et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to align the first chip and the second chip of Cho and Lin et al. in direction of bend, such as taught by Chang et al. depending on the desired configuration of the design.

Response to Arguments

4. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

March 17, 2005

Hung Vu

Primary Examiner